

FIG. 1A

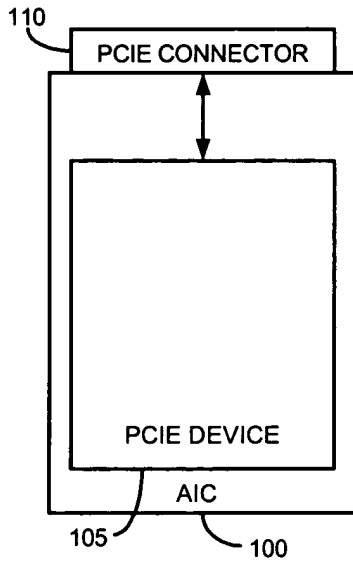


FIG. 1B

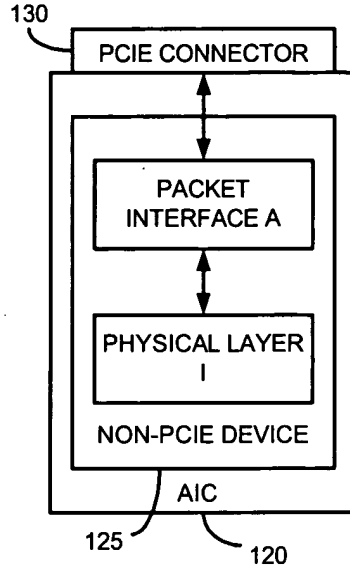


FIG. 1C

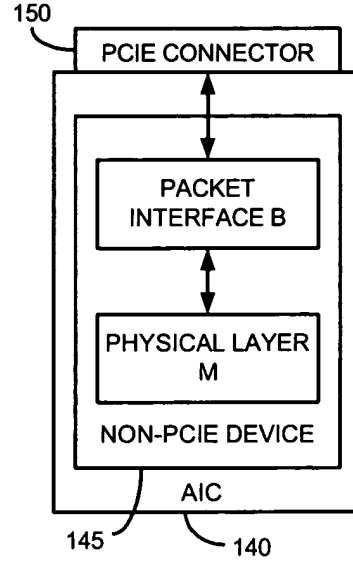


FIG. 3A

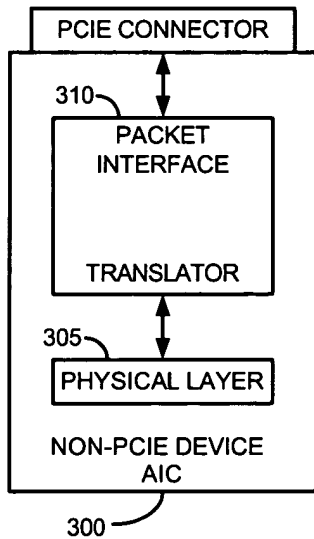


FIG. 3B

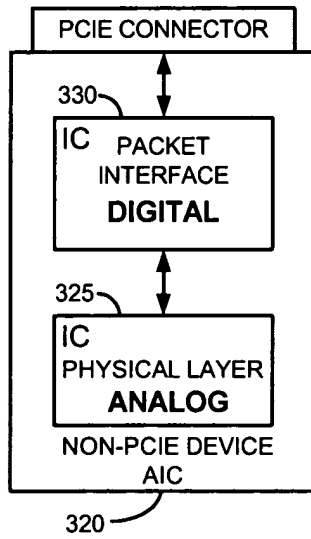


FIG. 3C

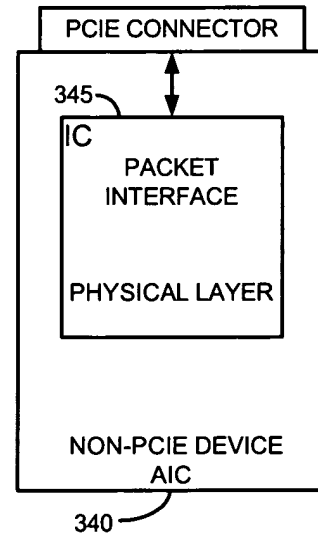


FIG. 2

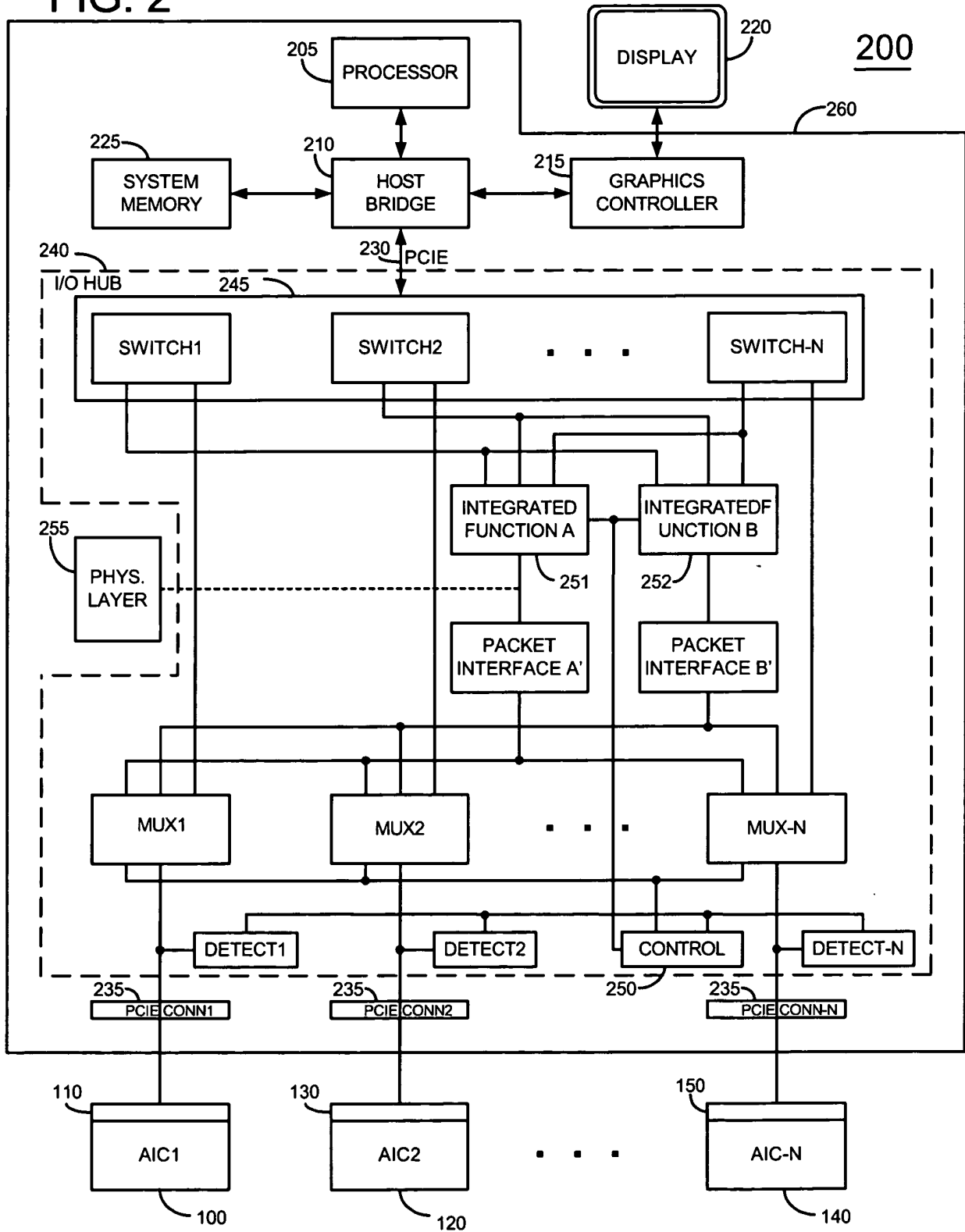


FIG. 4 is a block diagram of a system 400. The system 400 includes a host system and an I/O HUB 240. The host system includes a PROCESSOR 205, SYSTEM MEMORY 225, HOST BRIDGE 210, DISPLAY 220, and GRAPHICS CONTROLLER 215. The I/O HUB 240 includes SWITCH1, SWITCH2, ..., SWITCH-N, a PHYS. LAYER 255, and various integrated functions (FIXED INTEGRATED FUNCTION A, PROG. INTEG. FUNCTION, M) and packet interfaces (PACKET INTERFACE A', PACKET INTERFACE B'). The I/O HUB 240 is connected to multiple AICs (110, 130, ..., 150) via PCIE CONN1, PCIE CONN2, ..., PCIE CONN-N. The AICs are connected to a common bus 100. The I/O HUB 240 also includes MUX1, MUX2, ..., MUX-N and DETECT1, DETECT2, ..., DETECT-N blocks.

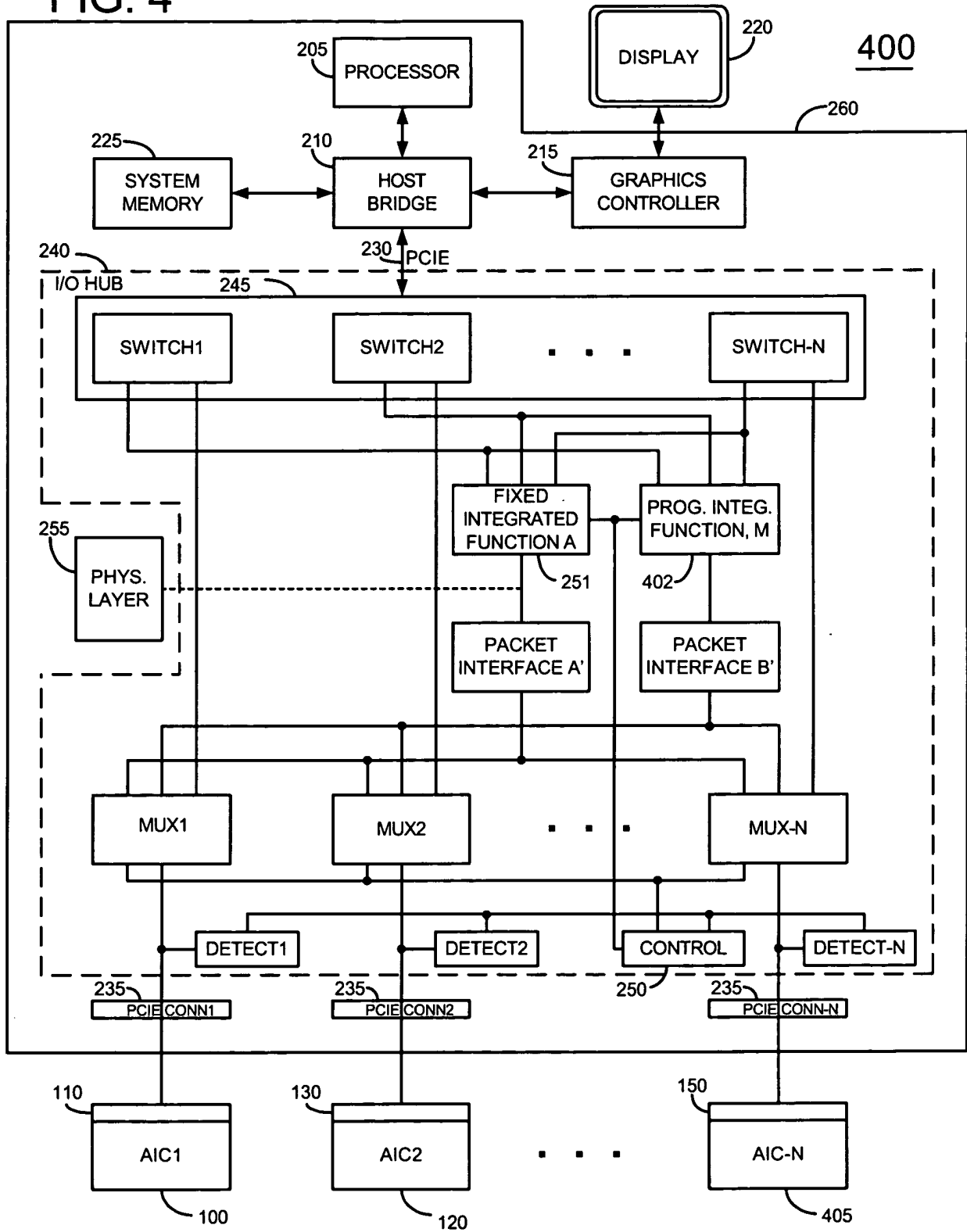


FIG. 5

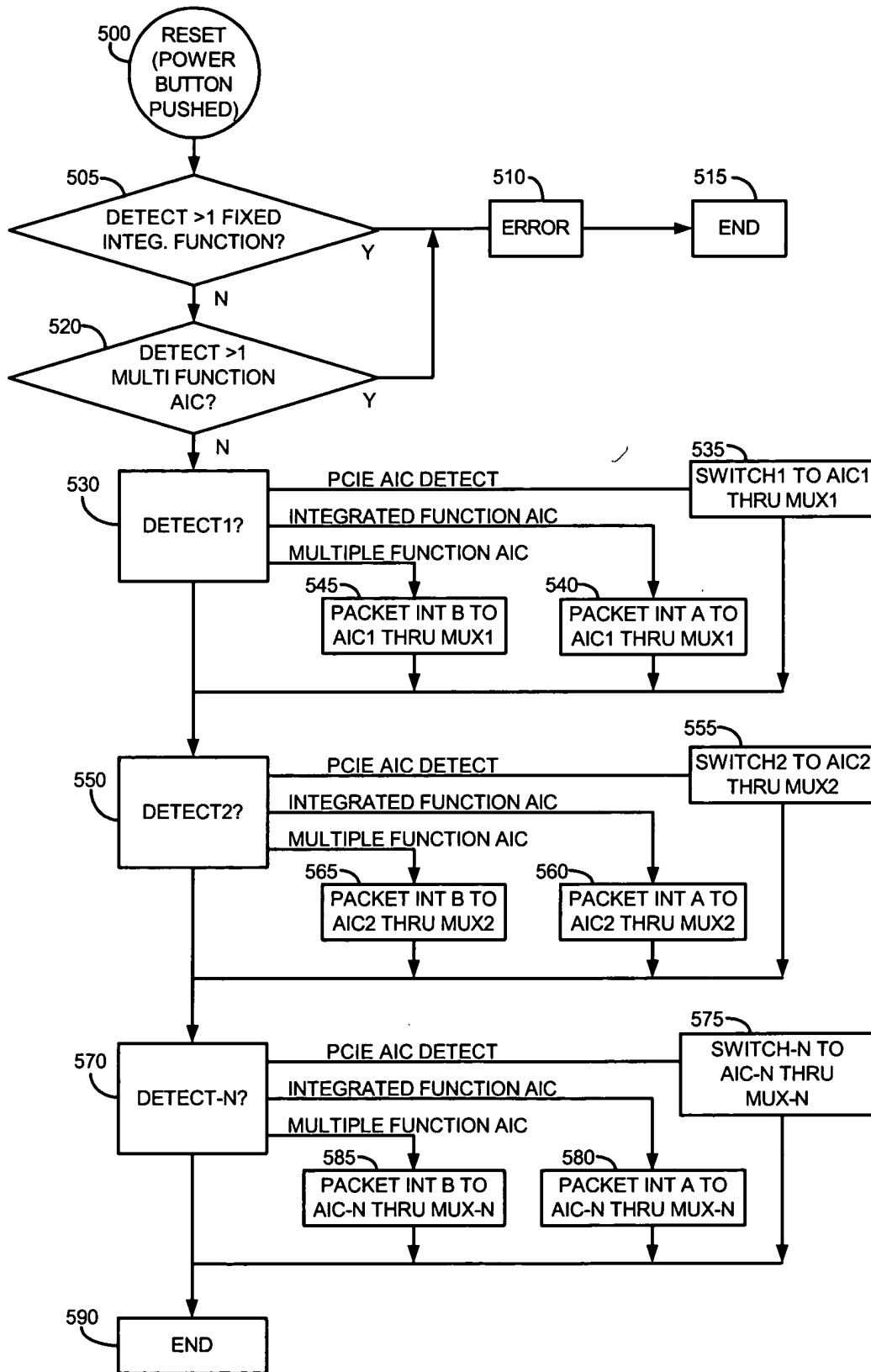


FIG. 6A

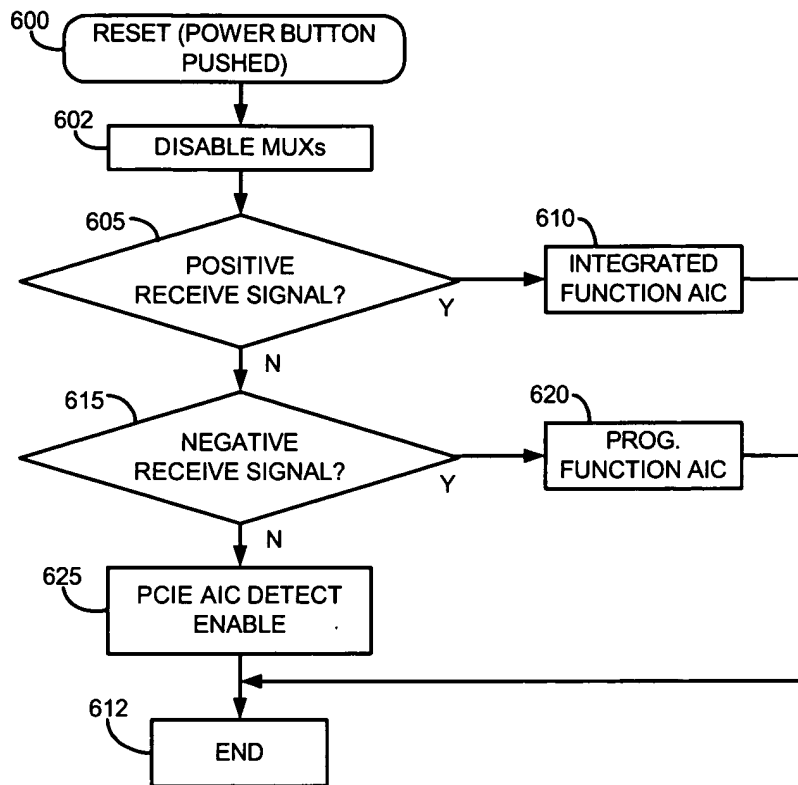


FIG. 6B

